Characterization and Recovery of Deep Sub Micron (DSM) Technologies Behavior Under Radiation

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Abstract—This paper serves as a twofold purpose: characterize the behavior of a reconfigurable chip exposed to radiation; and demonstrate a method for functionality recovery due to Total Ionizing Dose (TID) effects. The experiments are performed using a JPL-developed reconfigurable device, a Field Programmable Transistor Array (FPTA). The paper initially describes experiments on the characterization of the NMOS transistor behavior for TID values up to 300krad. The behavior of analog and digital circuits downloaded onto the FPTA chip is also assessed for TID effects. This paper also presents a novel approach for circuit functionality recovery due to radiation effects based on Evolvable Hardware. The key idea is to reconfigure a programmable device, in-situ, to compensate, or bypass its degraded or damaged components. Experiments with total radiation dose up to 300kRad show that while the functionality of a variety of circuits is degraded/lost at levels before 200kRad, the correct functionality can be recovered through the proposed evolutionary approach, and the chips are able to survive higher radiation, for several functions in excess of total radiation dose of 250kRad.

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1. INTRODUCTION

Evolvable Hardware (EHW) provides a new methodology for circuit design and self-recovery. Currently most electronic circuits are engineered once to perform a certain task under well-known conditions. However, in the context of space exploration, conditions are never guaranteed. A spacecraft on a long-range mission can travel for years within our solar system, during which is put through a myriad of harsh and unpredictable conditions, such as radiation, temperature fluctuations, faults, and the degrading effects of age. Engineers can try to predict adverse conditions that the system may eventually be exposed to, but a failure to safeguard against any unforeseen fault will invariably compromise the functionality of the entire system.

In the context of a space mission to the outer planets lasting many years, the most prevalent problem is the exposure of the spacecraft to extremely high levels of radiation. Without the Earth protecting it, the spacecraft is essentially unshielded from the harsh radiation environment and is subjected to several sources of radiation, such as planetary Van Allen belts, solar winds, and particles trapped in the Jovian region. Radiation can cause a myriad of problems in the electronics of a spacecraft, such as individual bit "flips" in memory when a charged radiation particle hits an electronic storage element, and the more problem-some Single Event Latch-up (SEL), which causes a device component to draw excess current until it is shut down. SEL may also cause permanent damage. Finally,

exposure to radiation is a cumulative effect. In CMOS circuits, this means that charge is trapped in the oxide layer between the gate contact and the semiconductor substrate. This has a gradual effect of slowly changing each transistor's threshold voltage and I-V characteristics, eventually causing macroscopic change in the behavior of a circuit [1,2].

The above factors combine to form a significant design challenge to the engineer. In the traditional paradigm of electronic systems design, the engineer designs the system to withstand any foreseeable conditions that it may encounter. In addition to choosing system components that are suitable for the expected environments, NASA system engineers have traditionally used redundancy as a method to prevent failures. Redundancy involves the use of a plethora of backup systems such that if any critical system fails during the course of a spacecraft's flight, a ready made replacement would be ready to take its place. A 1994 JPL study of the critical telecommunication system on six prior missions (Voyager 1 and 2, Viking 1 and 2, Galileo, and Magellan) revealed that redundancy is likely to have saved five of these missions from catastrophic failure [3]. Redundancy however, requires the use of backup systems that have no discernable use while the primary systems are operational, and thus adds unbeneficial weight and power drain to the system.

Another technique for environments with high levels of radiation is the use of Radiation Hard technologies such as Silicon on Insulator (SOI), which allows compensating for the effect of radiation. However, the fabrication cost associated with extreme environment electronics is higher than Bulk CMOS. In this paper we will present another technique, based on Evolvable Hardware, for electronic survivability in high radiation environments.

A reconfigurable chip developed at JPL, the FPTA-2 chip, is used in the experiments described in this paper [4-6]. We submitted this chip to radiation using JPL facilities, applying a cumulative dose up to 300kRads. The behavior of NMOS transistors for different levels of radiation was measured in terms of IxV transfer function and threshold voltage. The response deterioration with radiation of both human designed and evolved circuits was also assessed. This paper also describes experiments in which the correct functionality of downloaded circuits are recovered using Evolutionary Algorithms. The Evolutionary Algorithms control the state of about 1,500 switches. Using a population of about 500 candidates and after running the Evolutionary process for about 200 generations, the correct functionality is recovered. Evolution is able to use the resources of the reconfigurable cells, even the radiation damaged components, to synthesize a new solution.

The results indicate that, using Evolvable Hardware technology, we can design and develop electronic components and systems that are inherently insensitive to radiation induced faults by using on-board evolution in hardware to achieve fault-tolerant and highly reliable systems. The long term results of the proposed research would allow electronics to adapt to an extreme environment and long mission duration.

The rest of this paper is structured as follows: Section 2 reviews the concept of evolutionary circuit design; Section 3 describes the overall system architecture, which include the Field Programmable Transistor Array (FPTA) device architecture. Section 4 describes the experimental setup. Section 5 describes measurements of NMOS transistor behavioral changes with radiation. Section 6 describes experiments on functionality recovery. Section 7 presents discussion on the results. Finally, the main conclusions of the work are listed in section 8.

2. EVOLUTIONARY CIRCUIT DESIGN

The idea behind evolutionary circuit synthesis/design and evolvable hardware (EHW) is to employ a genetic search/optimization algorithm that operates in the space of all possible circuits and determines solution circuits with desired functional response (here the word synthesis is used in most general sense). The genetic search is tightly coupled with a coded representation of the candidate circuits. Each circuit gets associated a "genetic code" or chromosome; the simplest representation of a chromosome is a binary string, a succession of 0s and 1s that encode a circuit. Synthesis is the search in the chromosome space for the solution corresponding to a circuit with a desired functional response. The genetic search follows a "generate and test" strategy: a population of candidate solutions is maintained each time; the corresponding circuits are then evaluated and the best candidates are selected and reproduced in a subsequent generation, until a performance goal is reached. In this project, since device models for radiation are not available, circuit evaluation is done directly in reconfigurable hardware, called *intrinsic*. More details on Evolutionary Circuit Design can be found in [4-8].

3. SYSTEM ARCHITECTURE

A complete stand-alone board-level evolvable system (SABLES) is built by integrating the FPTA and a DSP implementing the Evolutionary recovery algorithm, as shown in Figure 1. The system is connected to the PC only for the purpose of receiving specifications and communicating back the result of evolution for analysis. The system fits in a box 8" x 8" x 3". Communication between DSP and FPTA is very fast with a 32-bit bus operating at 7.5MHz. The FPTA can be attached to a Zif socket attached to a metal electronics board to perform extreme temperature and radiation experiments The

evaluation time depends on the tests performed on the circuit. Many of the tests attempted here require less than two milliseconds per individual, and runs of populations of 100 to 200 generations require only 20 seconds.

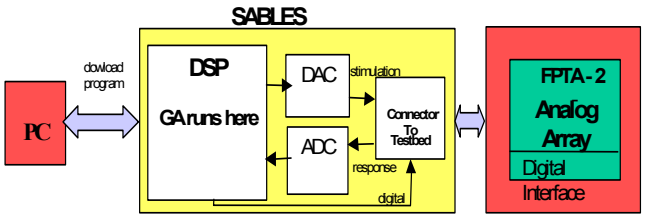

Figure 1: Complete System Architecture.

The FPTA is an evolution-oriented reconfigurable architecture (EORA). Important characteristics needed by evolution-oriented devices are *total accessibility*, needed in order to provide evolutionary algorithms the flexibility of testing in hardware any chromosomal arrangements, some of which may be dangerous for existing commercial devices (may lead to internal bus allocation conflicts and burn the chip) and thus forbidden, *granularity at low level* (here transistor) allowing evolution to choose/construct the most suitable building block for certain system, and *transparency,* which enables users to have access to internal device information, etc.

The FPTA has a configurable granularity at the transistor level. It can map analog, digital and mixed signal circuits. The architecture is cellular, with each cell having a set of transistors, which can be interconnected by other "configuration transistors". For brevity, the "configuration transistors" are called switches. However, unlike conventional switches, these can be controlled for partial opening, with appropriate voltage control on the gates, thus allowing for transistor-resistor type topologies.

The architecture of the FPTA consists of an 8x8 array of re-configurable cells. Each cell has a transistor array as well as a set of programmable resources, including programmable resistors and static capacitors. Figure 2 provides a detailed view of the FPTA cell. The re-configurable circuitry consists of 14 transistors connected through 44 switches. The status of the switches (ON or OFF) determines a circuit topology and consequently a specific response. Thus, the topology can be considered as a function of switch states, and can be represented by a binary sequence, such as "1011…", where a '1' is associated to a switch turned ON and a '0' to a switch turned OFF.

The re-configurable circuitry is able to implement different building blocks for analog processing, such as two and three stages OpAmps, logarithmic photo detectors, or Gaussian computational circuits. It includes three capacitors, Cm1, Cm2 and Cc, of 100fF, 100fF and 5pF respectively. Control signals come on the 9-bit address bus and 16-bit data bus, and access each individual cell providing the addressing mechanism for downloading the bit-string configuration of each cell. A total of ~5000 bits is used to program the whole chip. The pattern of interconnection between cells is similar to the one used in commercial FPGAs: each cell interconnects with its north, south, east and west neighbors. This is the first mixed-signal programmable array, FPMA, in the sense that its cells can be configured as both analog and digital circuitry; with its 64 cells it can configure more Operational Amplifiers (OpAmps) than the largest commercial Field Programmable Analog Array (FPAA) chip (which contains only 20 OpAmps). The chip was fabricated using a 0.l8u feature size technology.

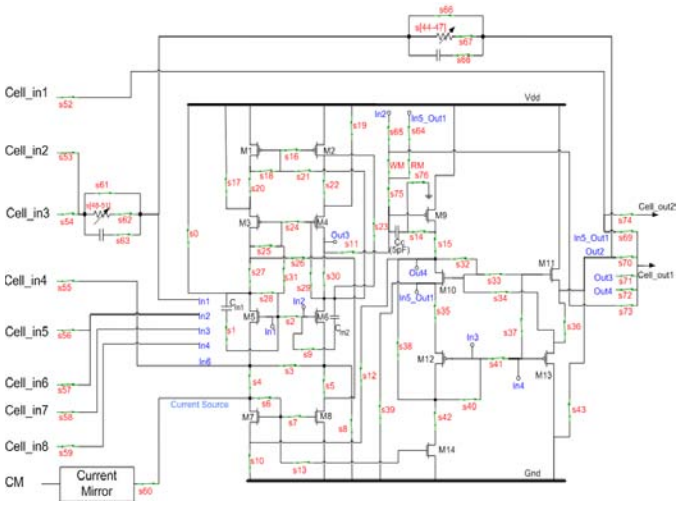

Figure 2: FPTA cell topology

The rationale of the Evolvable Hardware approach is to mitigate drifts, degradation, or damage on electronic devices in extreme environments by using re-configurable devices and adaptive self-reconfiguration of the circuit topology. Normally circuits are designed to exploit device characteristics within certain temperature/radiation range; when that is exceeded, the circuit function gradually degrades. In the case of reconfigurable devices, although the device parameters change in extreme environments, a new circuit design, suitable for new parameters, may be mapped into the reconfigurable device to reproduce the initial circuit function. Several search techniques can be used to find those circuit solutions for extreme environment. Evolutionary Algorithms are particularly efficient search techniques for the large search spaces generated when programming re-configurable chips such as the FPTA. The new designs, suitable for various environmental conditions, can be determined prior to operation (flight) or determined in-situ by reconfiguration or Evolutionary Algorithms. In-situ device reconfiguration with Evolutionary Algorithms is

an effective technique, because the combined effects of radiation and temperature on the devices is hard to model.

4. Radiation Experiment and Setups

We conducted the radiation experiments over the course of 180 hours starting from Aug. 18 2004 (Figure 3). The radiation experiment conducted followed the radiation and test methodology first described in [8], with the difference being a larger focus on the quantitative aspects of the change in individual NMOS and PMOS transistors and how that affects behavior at the circuit level. Test transistors were provided in the layout for behavior characterization under radiation. These test transistors are created on the same process as the rest of the transistors in the FPTA-2 cells and are thus assumed to behave similarly. If the radiation beam is homogenous across the transistor, we can further assume that the radiation affects the transistors in the cells in a similar way to the test transistors. Since radiation is a cumulative effect, we were particularly interested in the Total Ionizing Dose (TID) effect of radiation on the transistor and circuit levels.

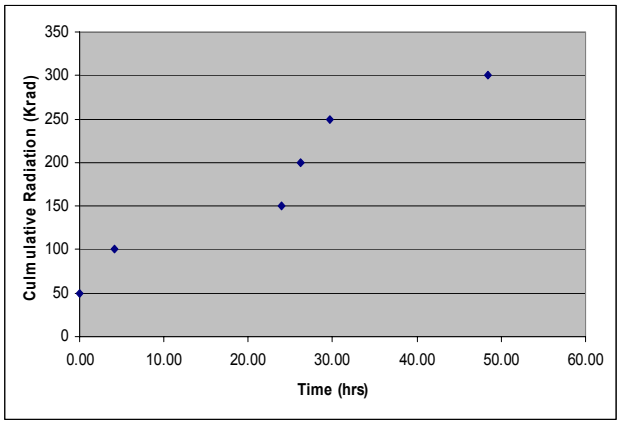

Figure 3: Cumulative Radiation Graph

Our radiation experiments were conducted at the JPL radiation facility. This radiation setup differed from earlier EHW radiation tests [8] in that for this test we used Cobalt 60 sourced gamma rays instead of the electron beam used previously. Compared to the radiation offered by electron beams and protons, Cobalt 60 gamma rays are significantly higher energy and much more penetrating. Logistically, the test involved placing a FPTA chip and its associated host board 28.5 cm away from a shielded Cobalt 60 source. The host board was included to provide easy biasing. When exposed at that distance, the Cobalt 60 source subjects the chip to 50 rad/sec of gamma ray radiation. FPTA chips were radiated under both biased (power on) and unbiased (power off) conditions. The biasing scheme promotes ionization by introducing a potential difference across the inputs and outputs and thus facilitating the trapping of charge. The biasing scheme is shown in Figure 4, with input at Vdd and outputs grounded.

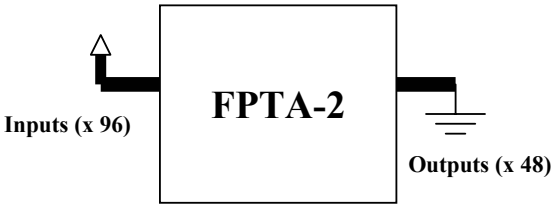

Figure 4: Biasing scheme of the FPTA.

5. Transistor Characterization

After irradiation, we measured the I-V, drain current versus gate voltage (Id vs. Vg) and threshold (Vth) characteristics using an Agilent 4155B semiconductor parameterization device. Vth characterization was done according to the application note in [9]. Id vs. Vg characteristics were measured with the setup indicated in Figure 5.

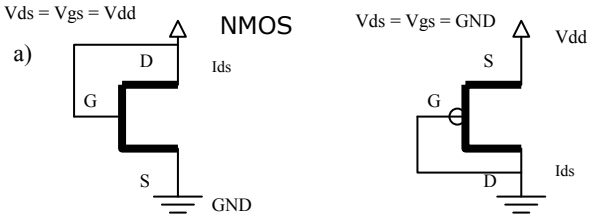

Figure 5: MOS transistors setup for Id x Vg characterization.

Figure 6 displays the change in the threshold voltage for two MOS transistors N2 (W/L = 0.54u/0.27u) and N3 (W/L = 0.72u/0.36u). Figure 7 shows the the I-V curve (drain current x gate voltage) for different radiation levels. PMOS transistor behavior has also been characterized in the same way.

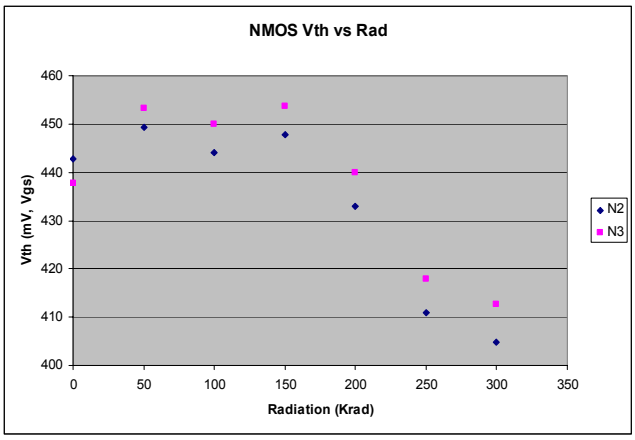

Figure 6: Graph of Vth with radiation on two NMOS

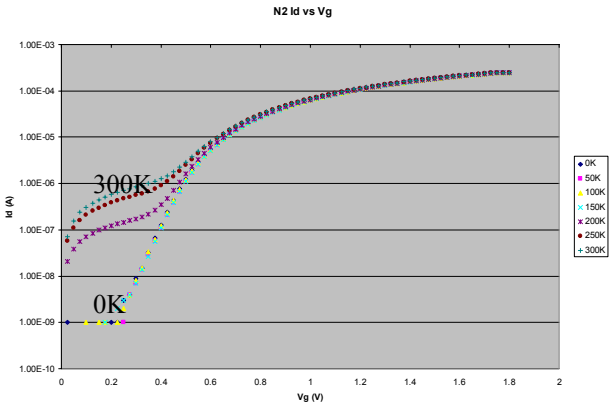

Figure 7: NMOS Gate voltage vs. Drain current on a logarithmic scale

The overall results from these experiments very closely conformed to what was expected based on literature in this field and the results of our previous experiments with evolutionary algorithms [8]. A clear link between the shifts in the NMOS threshold voltage (Vth) and Id vs. Vg and qualitative distortion in the behavior of the downloaded circuit functions can easily be seen in the biased chip (next section).

6. Recovery Experiments

We present results on the recovery of the following circuits downloaded onto the FPTA: Inverter; half-wave rectifier, NAND gate and digital to analog converter. The recovery of Evolution was, in general, successful in improving the response of degraded circuits.

6.1 – Inverter

A conventional digital inverter was mapped and downloaded onto one FPTA cell. Figure 8 depicts the schematic of a digital inverter. Figure 9 shows the response of the downloaded circuit without radiation. The input signal is a ramp.

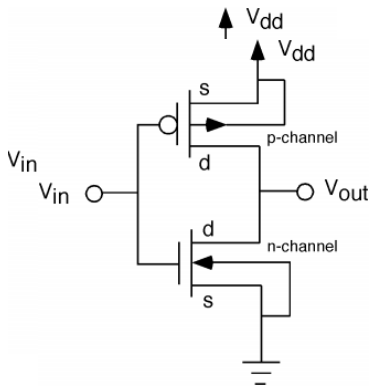

Figure 8: CMOS Inverter

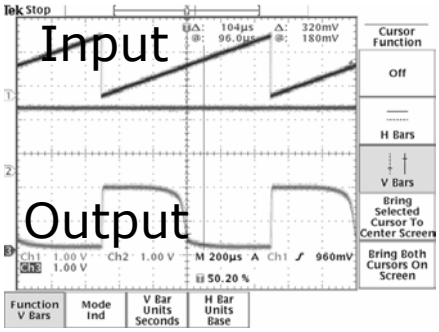

Figure 9: Input and Output waveforms for the Inverter circuit without radiation.

The circuit output slightly changes when radiation is applied. Figure 10 depicts the circuit response for 300Krad. The circuit output is still correct for this radiation level, nevertheless it can be seen that the output transition voltage shifts slightly to the left (outputs switches from '1' to '0' at a lower value of the input).

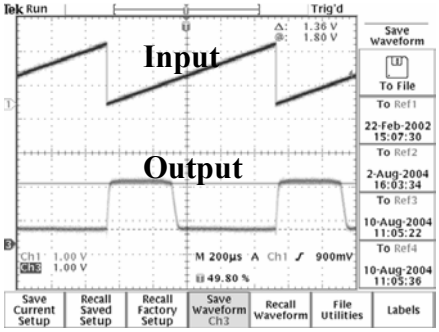

Figure 10: Input and Output waveforms for the Inverter circuit for 300Krad.

An approximate transistor simulation model for radiation can be obtained by changing the threshold voltage according to the behavior shown when characterizing the transistor behavior for radiation. From Figure 6 it can be seen that NMOS threshold voltage reduces for 300Krad. PMOS transistors on the other hand did not show a meaningful change in the threshold voltage at 300Krad. A

digital inverter was simulated incorporating these changes in the transistor model and the results are similar to the one shown in Figure 10. As we reduce the NMOS transistor threshold voltage (higher radiation levels), the output transition voltage also shifts to the left, as shown in Figure 11.

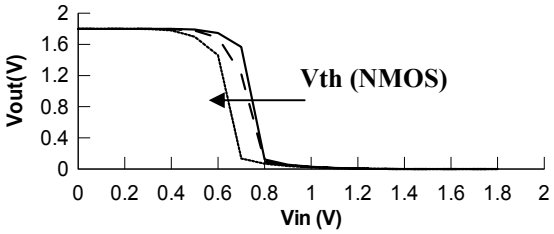

Figure 11: Output waveform for a digital inverter in simulation. From the right to the left the NMOS transistor threshold voltage gets lower.

6.2- Half-Wave Rectifier

Figure 12 shows the response of an evolved half-wave rectifier circuit before the chip was submitted to radiation.

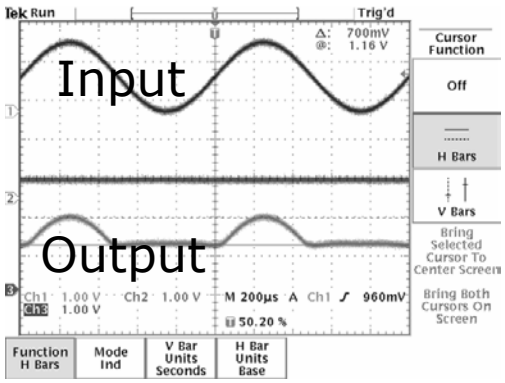

Figure 12: Response of the half-wave rectifier circuit before radiation was applied to the chip.

It was observed no change in the behavior of the circuit for TID levels up to 200Krad. This was consistent with the graph of Figure 6, which shows that the NMOS threshold voltage value has noticeable change starting at 200Krad. Figure 13 shows the slightly degraded half-wave rectifier response at 200Krad.

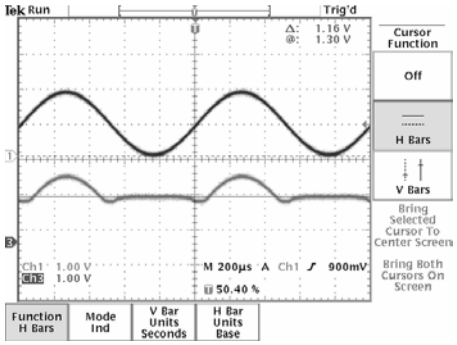

Figure 13: Half-Wave rectifier response at 200Krad.

As expected from the graph of Figure 6, as the TID reaches 300Krad, the circuit response deteriorates even further. Figure 14 depicts the degraded response at 300Krad and the response of the recovered circuit obtained through evolution.

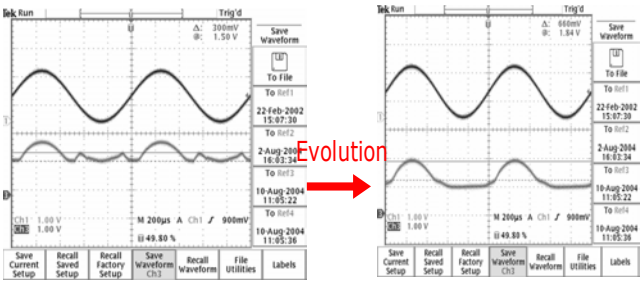

Figure 14: Response of the Rectifier circuit after being radiated to 300kRads resulting in deterioration (left) through loss of rectification, followed by recovery through Evolution (right).

The circuit recovery was performed after a 5 minute execution of evolutionary algorithm, sampling 200 individuals over 100 generations.

6.3- NAND Gate

Both a human designed and an evolved NAND gate were downloaded onto the FPTA and their behavior measured for radiation effects. Figure 15 presents the behavior of the human designed NAND gate at 50Krad and 300Krad. Figure 16 shows the same for the evolved NAND gate.

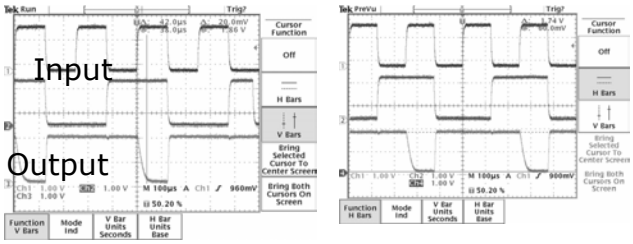

Figure 15: Human designed NAND behavior at 50Krad (left) and 300Krad (right).

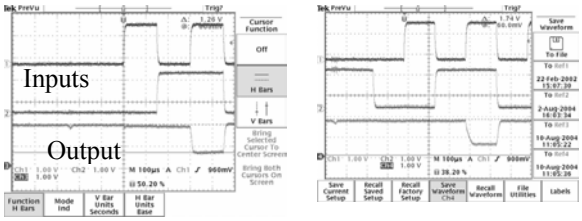

Figure 16: Evolved NAND behavior at 50Krad (left) and 300Krad (right).

Figures 15 and 16 show that both the human designed and the evolved NAND gates are robust to TID until 300kRad. This result is somewhat expected, since digital circuits are usually more robust to component drifts (as caused by radiation) than analog circuits. No recovery was needed in this case study.

6.4- Digital to Analog Converter (DAC)

A 4-bit DAC was hierarchically evolved from a 3-bit DAC previously evolved [4]. Figure 17 shows the circuit response without radiation effects.

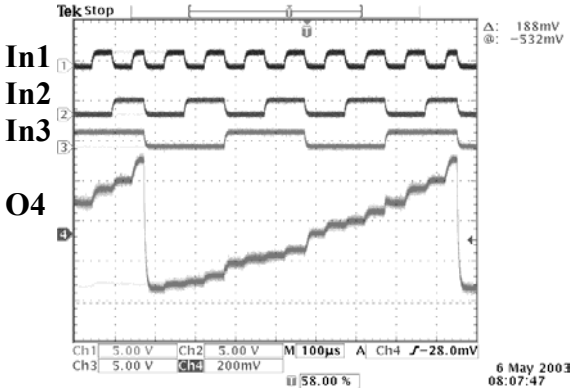

Figure 17. Evolved 4-bit DAC inputs (In1, In2 and In3) and output (O4). MSB (In4) not included due to limitation in the number of oscilloscope channels.

Figure 18 depicts the degraded circuit response at 175Krad and the recovered circuit response. Figures 19 presents the same information for 250Krad.

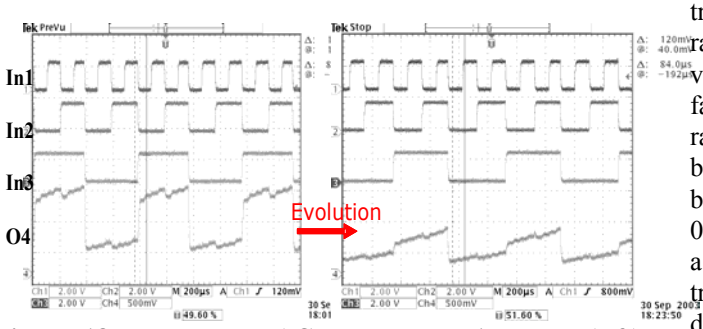

Figure 18: Degraded DAC response at 175Krad (left) and recovery by evolution (right).

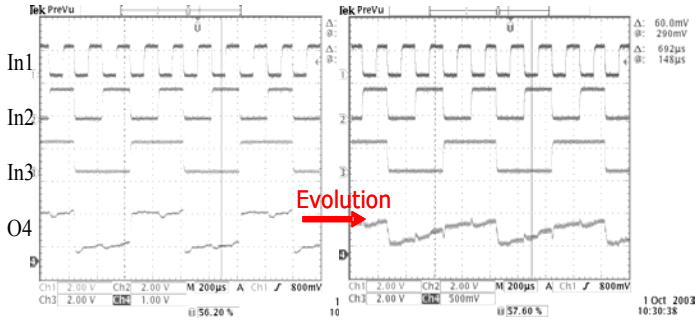

Figure 19: Degraded DAC response at 250Krad (left) and recovery by evolution (right).

Since the DAC is a more sensitive (LSB is 28mV) circuit, even small changes in the transistor threshold voltage at 175Krad already affect the circuit response. It can be verified that the circuit exhibited only slight improvement after evolution for both radiation levels. This was probably because of failure due to radiation of the 3-bit DAC building block itself. In order to improve the recovery, a new 3-bit DAC for the damaged FPTA should be evolved, and used for the evolution of the 4-bit DAC.

7. DISCUSSION

The lack of the expected complete failure of the chip at high levels of irradiation can be explained by our use of gamma rays. While gamma rays are higher energy and significantly more penetrating than electron or proton radiation, it is much less ionizing. Gamma rays are a form of electromagnetic radiation that is massless and chargeless and thus travel significantly farther through all types of matter. Ionization from gamma rays results indirectly from an interaction of a gamma ray photon with an electron, rather than through direct electron-electron or electron-proton interactions.

It is ionization and the amount of charge trapping that occurs in the oxide between metal and gate in a MOS transistor, not total radiation exposure, that causes MOS transistor parameter shifts. This explains the far smaller radiation effect on the transistor IV curve of gamma rays versus protons or electrons and subsequently, the far earlier failure of the FPTA chips when subjected to electron radiation versus Co-60 gamma rays [8]. This is illustrated by the difference between Figure 20 and Figure 7. While both show the same trend of a larger drain current at Vg = 0, the transistor under the X-ray source of Figure 20 reaches a flat line at 300 Krad, while the gamma ray exposed transistor of Figure 7 still has two orders of magnitude difference in current between Vg = 0 and Vg = 1.8 at 300Krad.

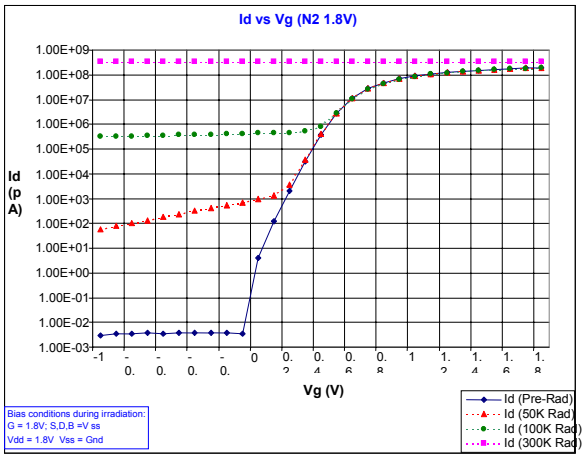

Figure 20: X-ray (electron) effects on IV curve [8]

8. CONCLUSION

This paper characterized the behavior of individual MOS transistors for TID until 300Krad. The link between Vth and I-V parameter shifts of individual transistors and qualitative circuit behavior was clearly evident. The ability of evolutionary algorithms to improve substantially deteriorated circuits without human intervention was once again demonstrated.

Gamma ray ionization effect on CMOS transistors has been documented to be fairly small in [11], requiring much longer radiation time to manifest effects that become apparent fairly early when using electron radiation. Since we were interested in Total *Ionization* Dose, a radiation source with low ionizing capabilities was not as effective as x-ray radiation sources used in previous experiments with the same chip [8].

In the future, more quantitative analysis of the behavior of circuits in relation to individual transistor parameter shifts would be a good direction to proceed. In the interests of efficiency, future radiation tests should be conducted with electrons or protons to truly gauge the ability of evolution to fix compromised circuits.

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